

FIG. 1A

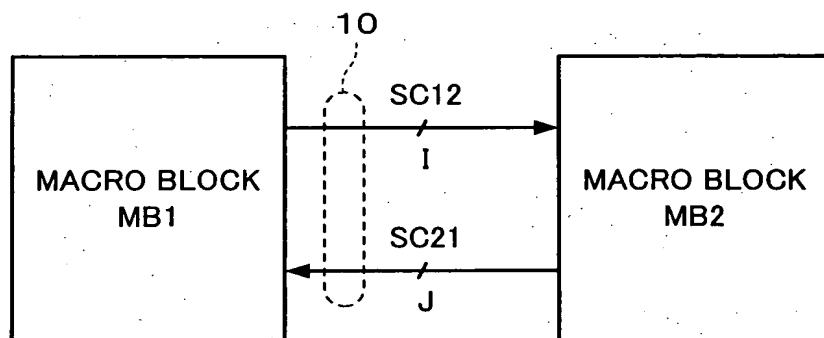


FIG. 1B

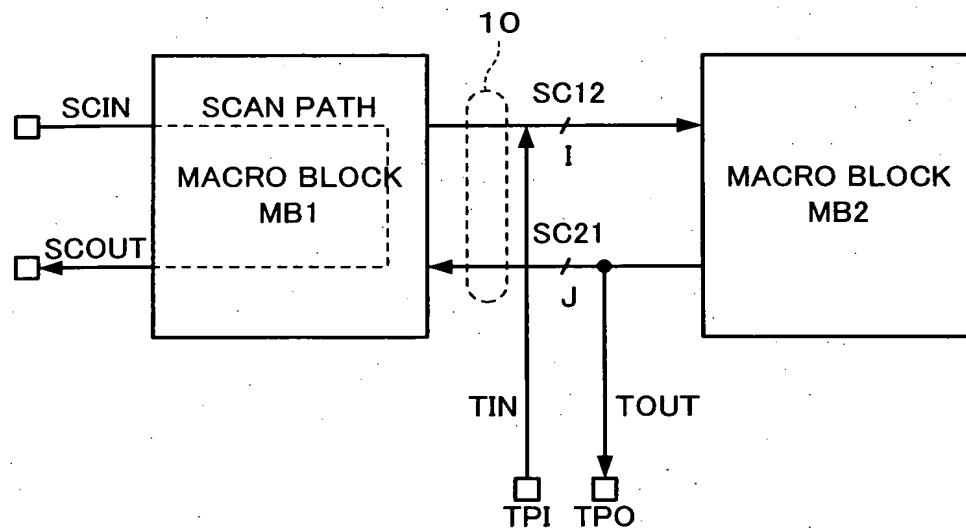


FIG. 2

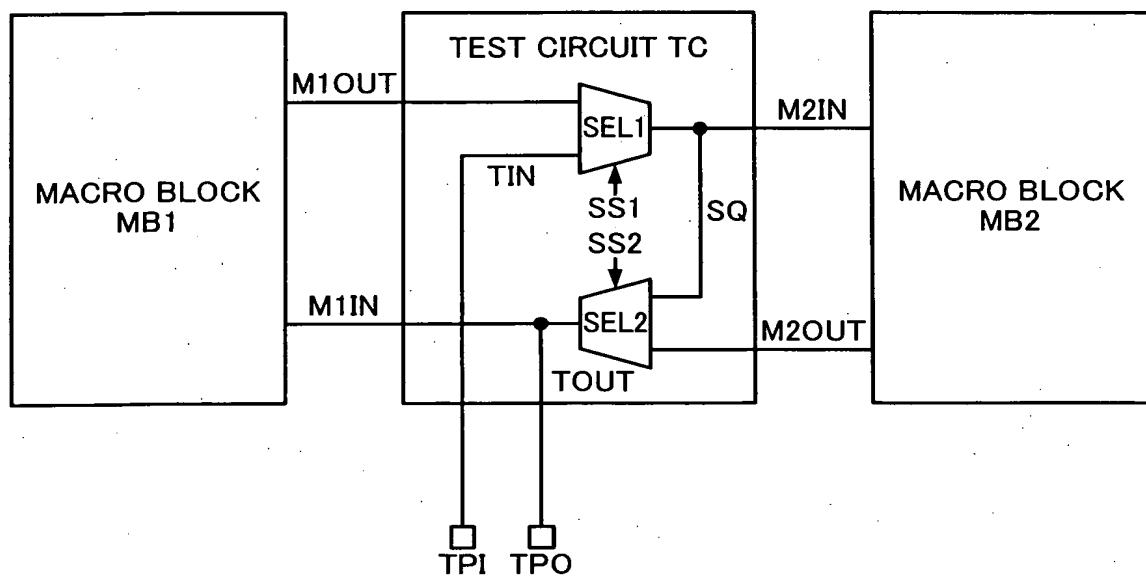


FIG. 3A FIRST TEST MODE

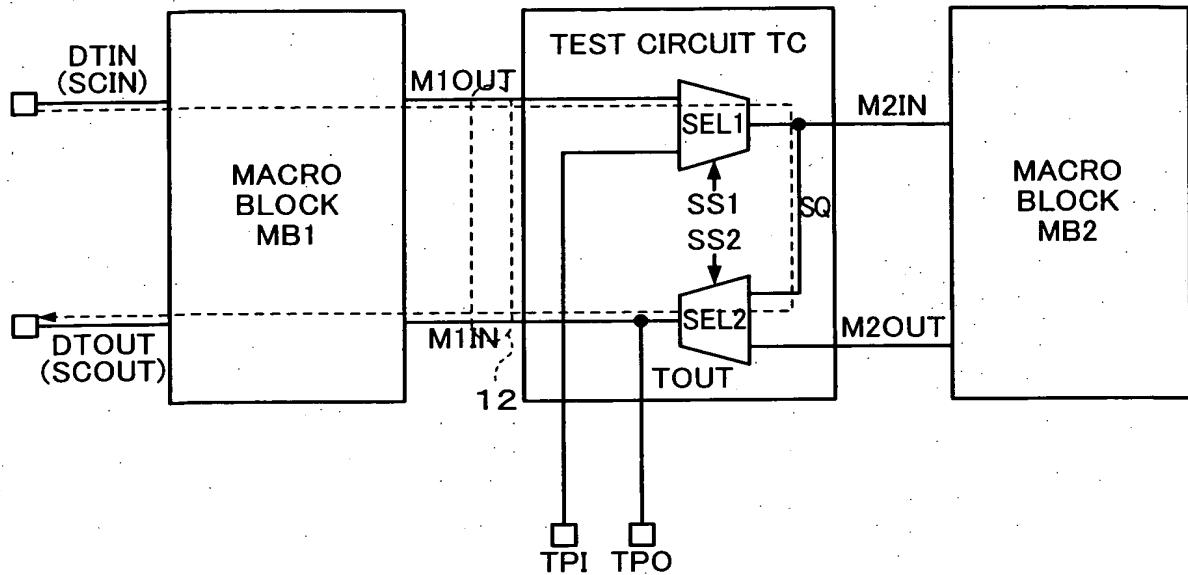


FIG. 3B SECOND TEST MODE

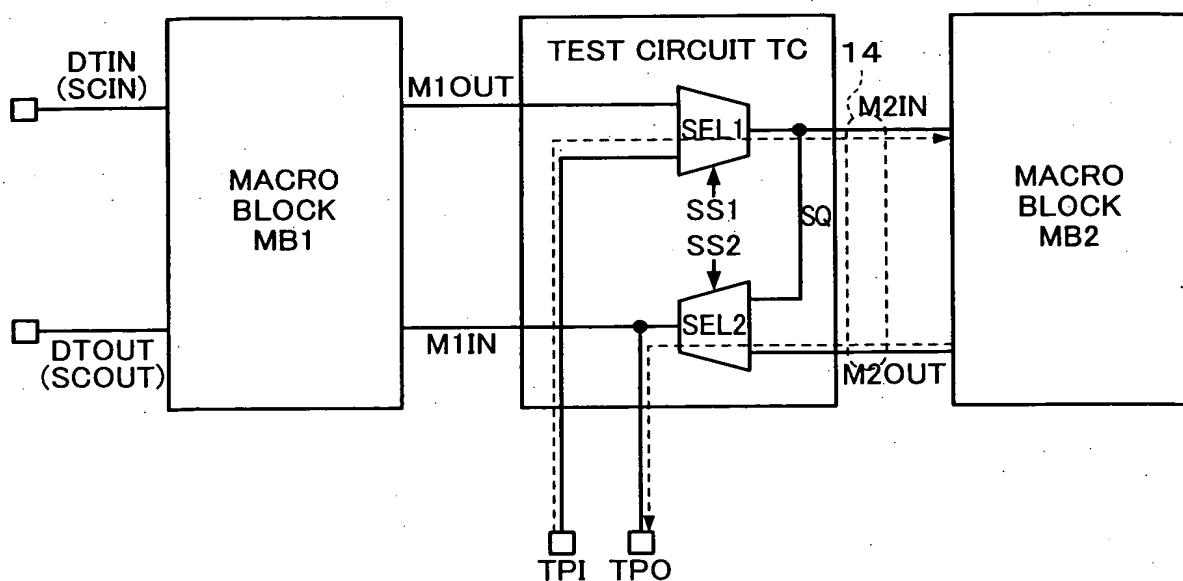


FIG. 4

SCAN PATH SETTING

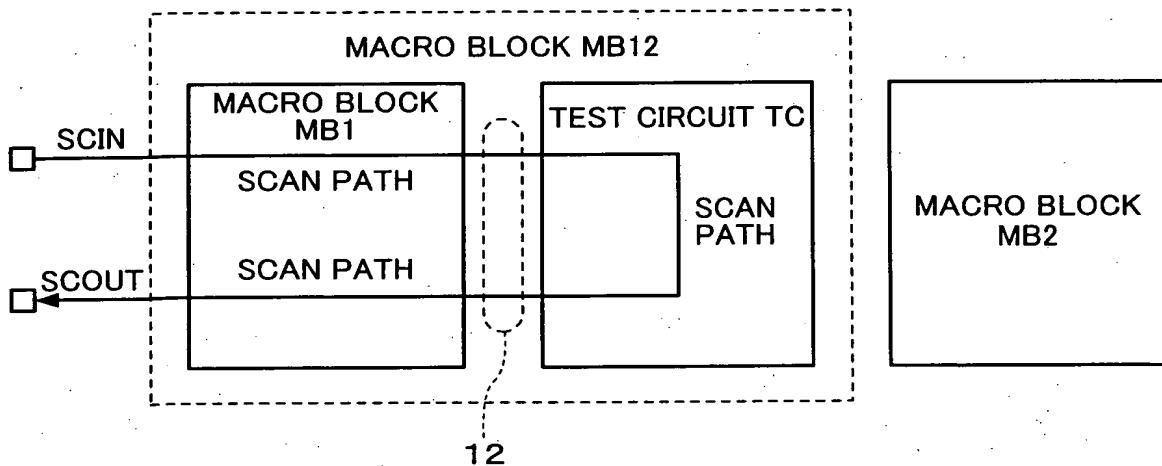


FIG. 5A

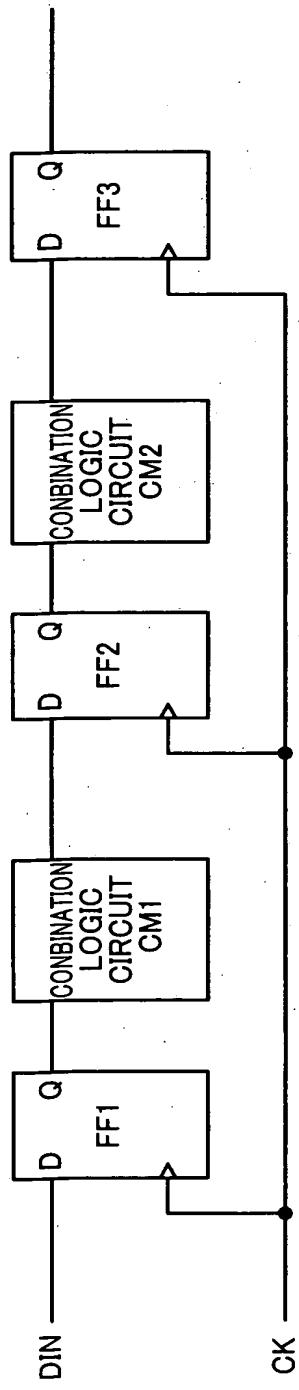


FIG. 5B

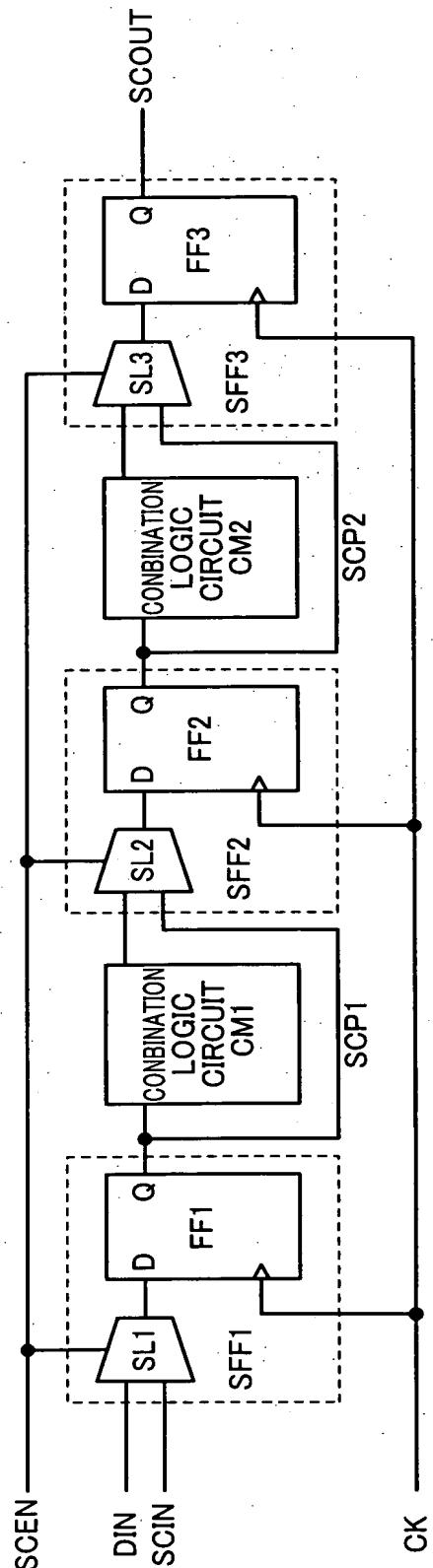
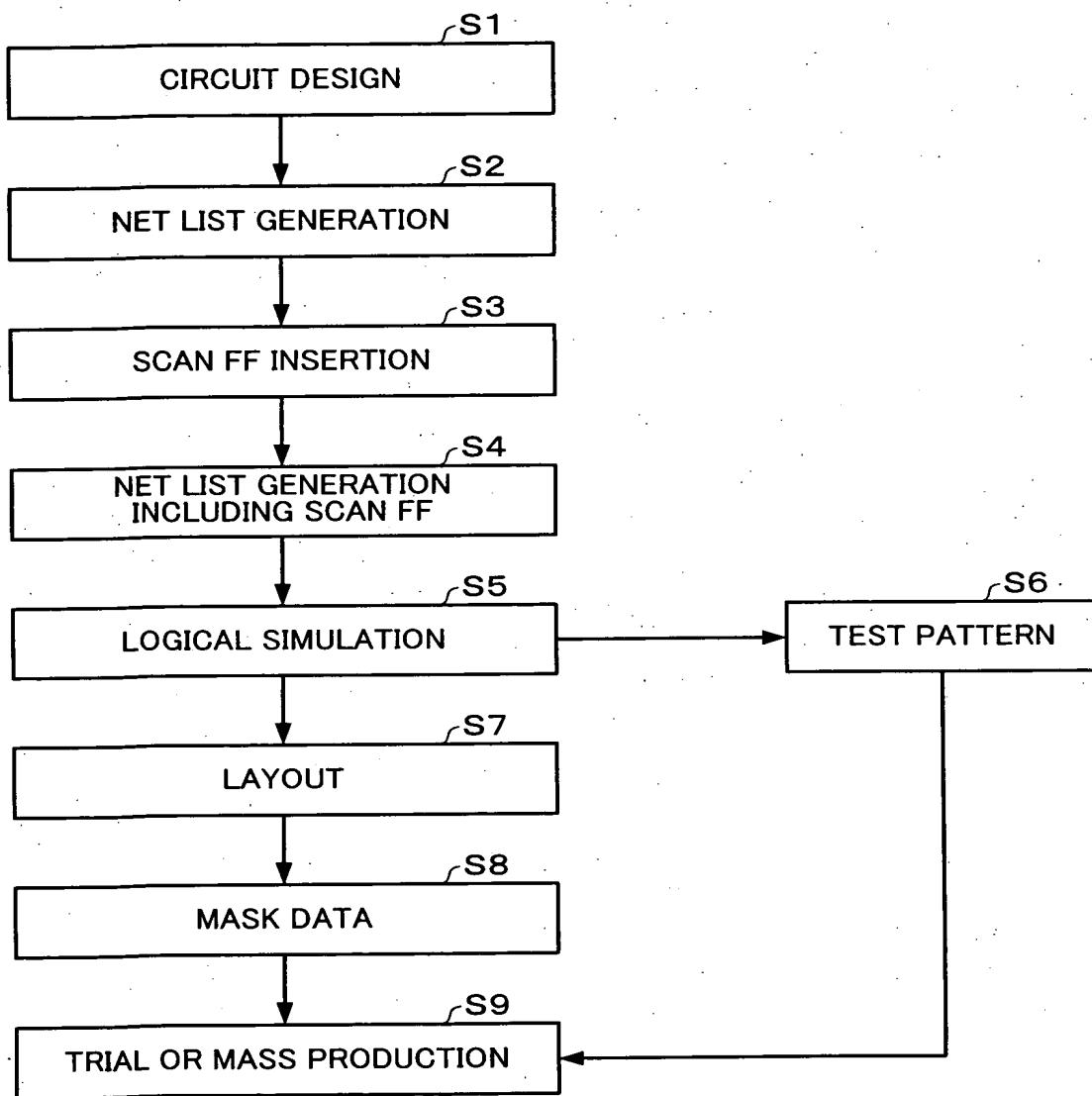


FIG. 6



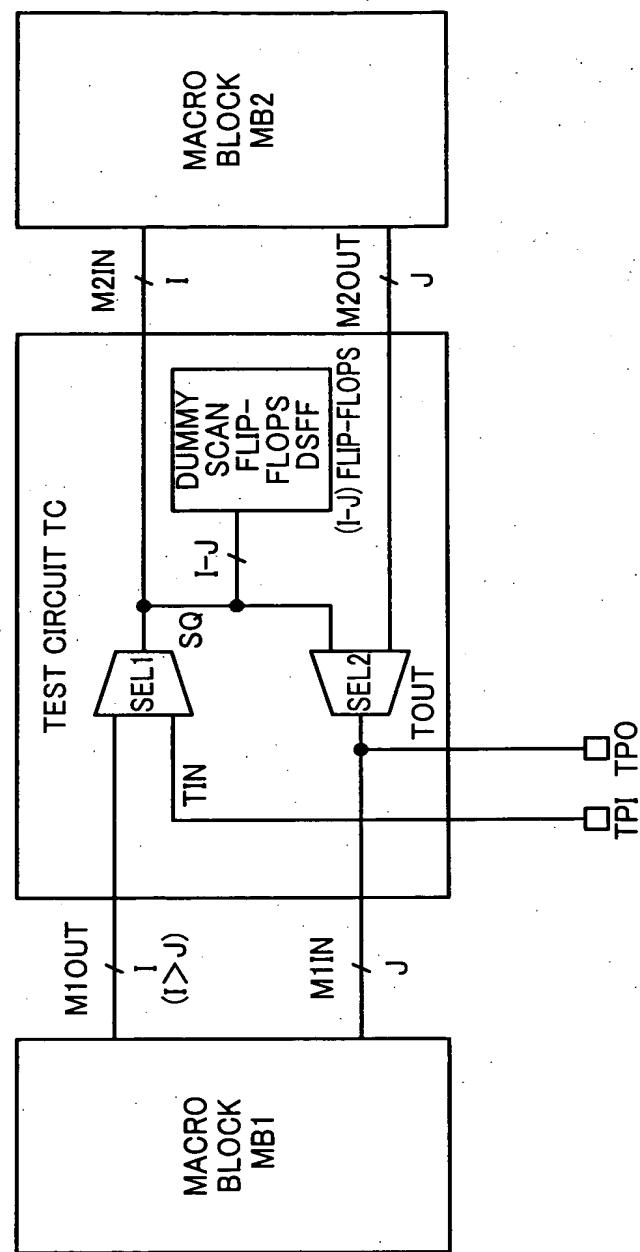


FIG. 7

FIG. 8A

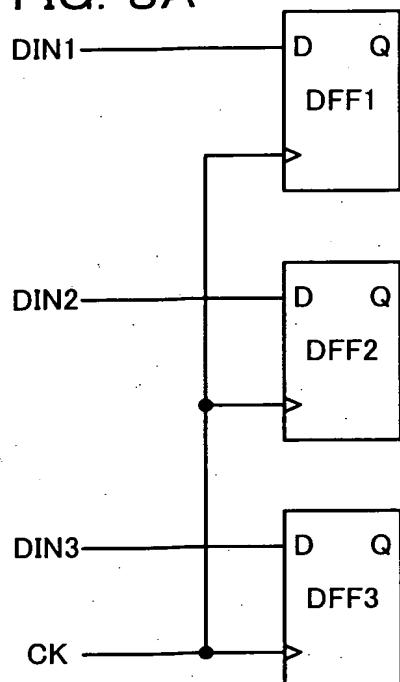


FIG. 8B

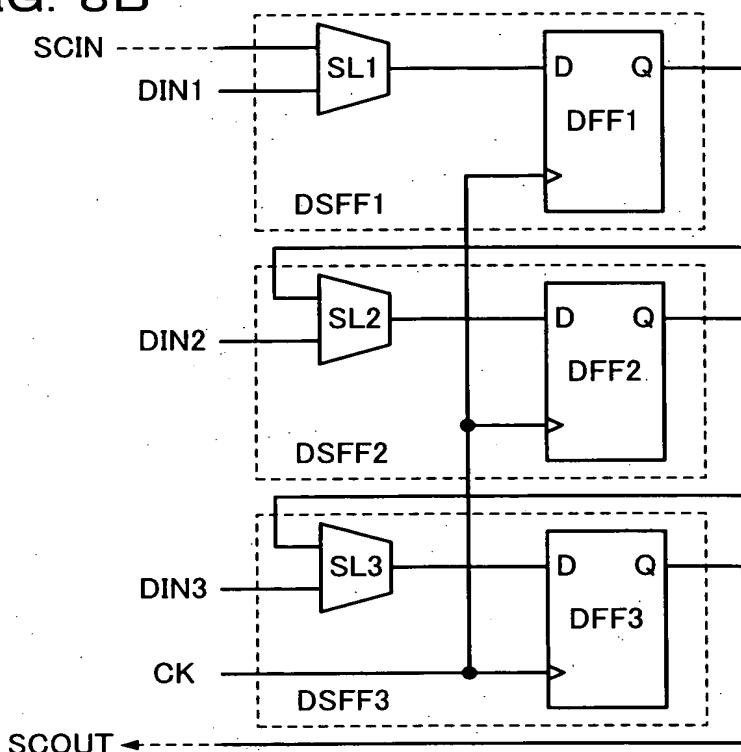


FIG. 8C

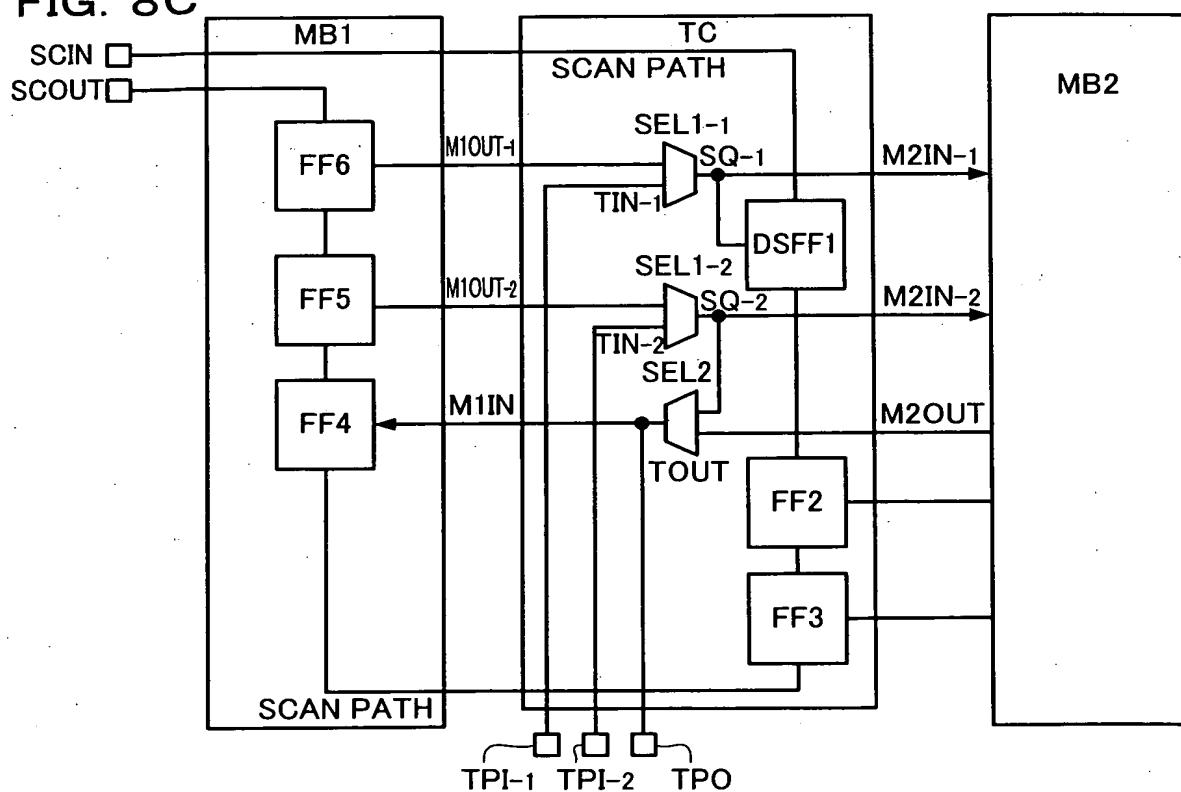


FIG. 9

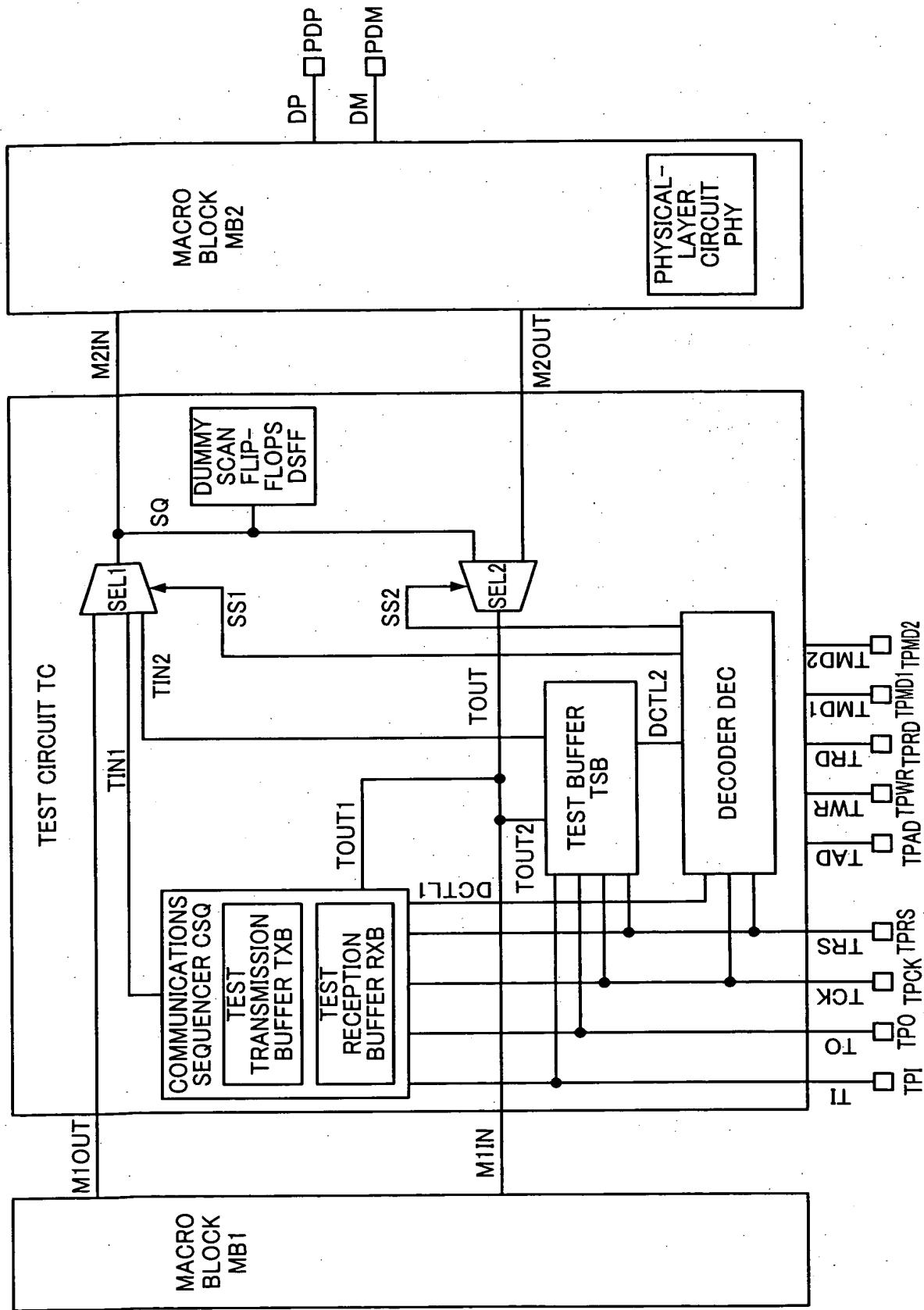


FIG. 10

TAD	TRD/TWR	Bit3	Bit2	Bit1	Bit0
0x0	W	TxBuf0[7]	TxBuf0[6]	TxBuf0[5]	TxBuf0[4]
0x0	R	RxBuf0[7]	RxBuf0[6]	RxBuf0[5]	RxBuf0[4]
0x1	W	TxBuf0[3]	TxBuf0[2]	TxBuf0[1]	TxBuf0[0]
0x1	R	RxBuf0[3]	RxBuf0[2]	RxBuf0[1]	RxBuf0[0]
0x2	W	TxBuf1[7]	TxBuf1[6]	TxBuf1[5]	TxBuf1[4]
0x2	R	RxBuf1[7]	RxBuf1[6]	RxBuf1[5]	RxBuf1[4]
0x3	W	TxBuf1[3]	TxBuf1[2]	TxBuf1[1]	TxBuf1[0]
0x3	R	RxBuf1[3]	RxBuf1[2]	RxBuf1[1]	RxBuf1[0]
0x4	W	TxBuf2[7]	TxBuf2[6]	TxBuf2[5]	TxBuf2[4]
0x4	R	RxBuf2[7]	RxBuf2[6]	RxBuf2[5]	RxBuf2[4]
0x5	W	TxBuf2[3]	TxBuf2[2]	TxBuf2[1]	TxBuf2[0]
0x5	R	RxBuf2[3]	RxBuf2[2]	RxBuf2[1]	RxBuf2[0]
0x6	W	TxBuf3[7]	TxBuf3[6]	TxBuf3[5]	TxBuf3[4]
0x6	R	RxBuf3[7]	RxBuf3[6]	RxBuf3[5]	RxBuf3[4]
0x7	W	TxBuf3[3]	TxBuf3[2]	TxBuf3[1]	TxBuf3[0]
0x7	R	RxBuf3[3]	RxBuf3[2]	RxBuf3[1]	RxBuf3[0]
0x8	R/W	-	-	TXMODE	-
0x9	R/W	XCVRSELECT	TERMSELECT	OPMODE1	OPMODE0
0xA	R/W	PLLSELECT	OSCENB	CLKSELECT1	CLKSELECT0
0xB	R/W	RESET	RAWCLOCK	ANA_IQ	SUSPEND
0xC	R/W	OPENLOOP	TgICLK	DivideCLK	MonCLK(R)
0xD	R	MonRXACTIVE	MonRXERROR	MonLINESTATE1	MonLINESTATE0
0xE	R/W	-	-	MonRXERROR(R)	LatRXERROR
0xF	R/W	-	-	-	TXSTART

FIG. 11A

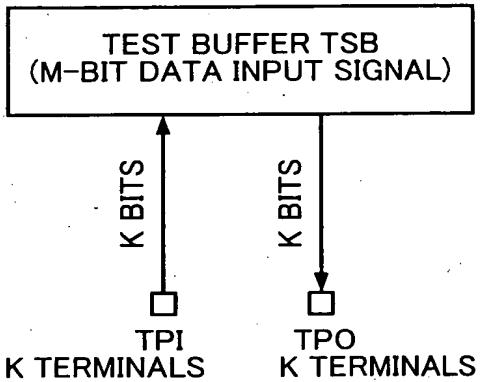


FIG. 11B

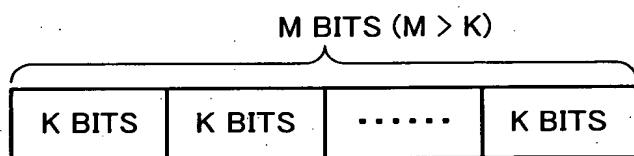


FIG. 11C

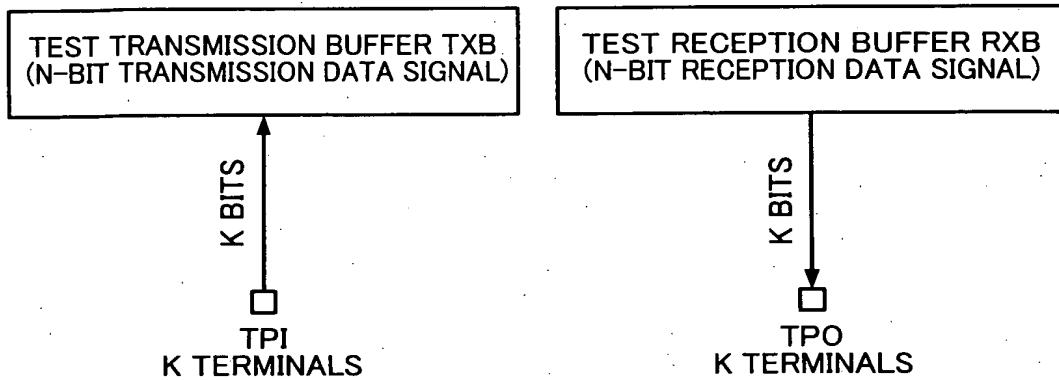


FIG. 11D

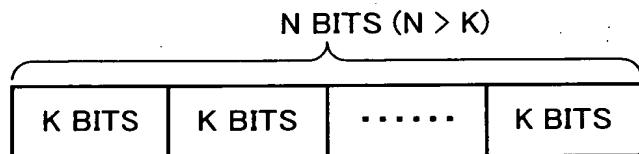


FIG. 12

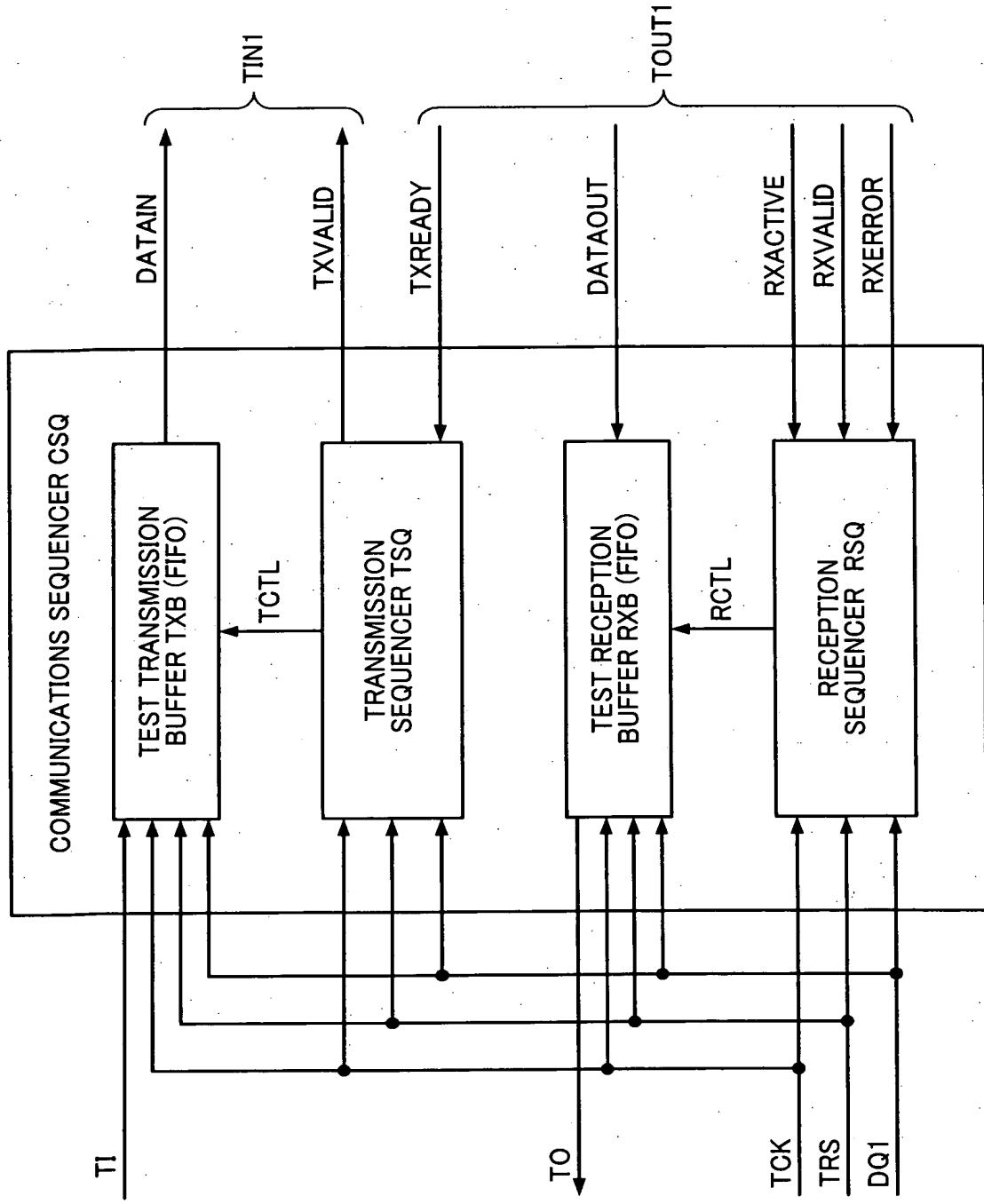


FIG. 13

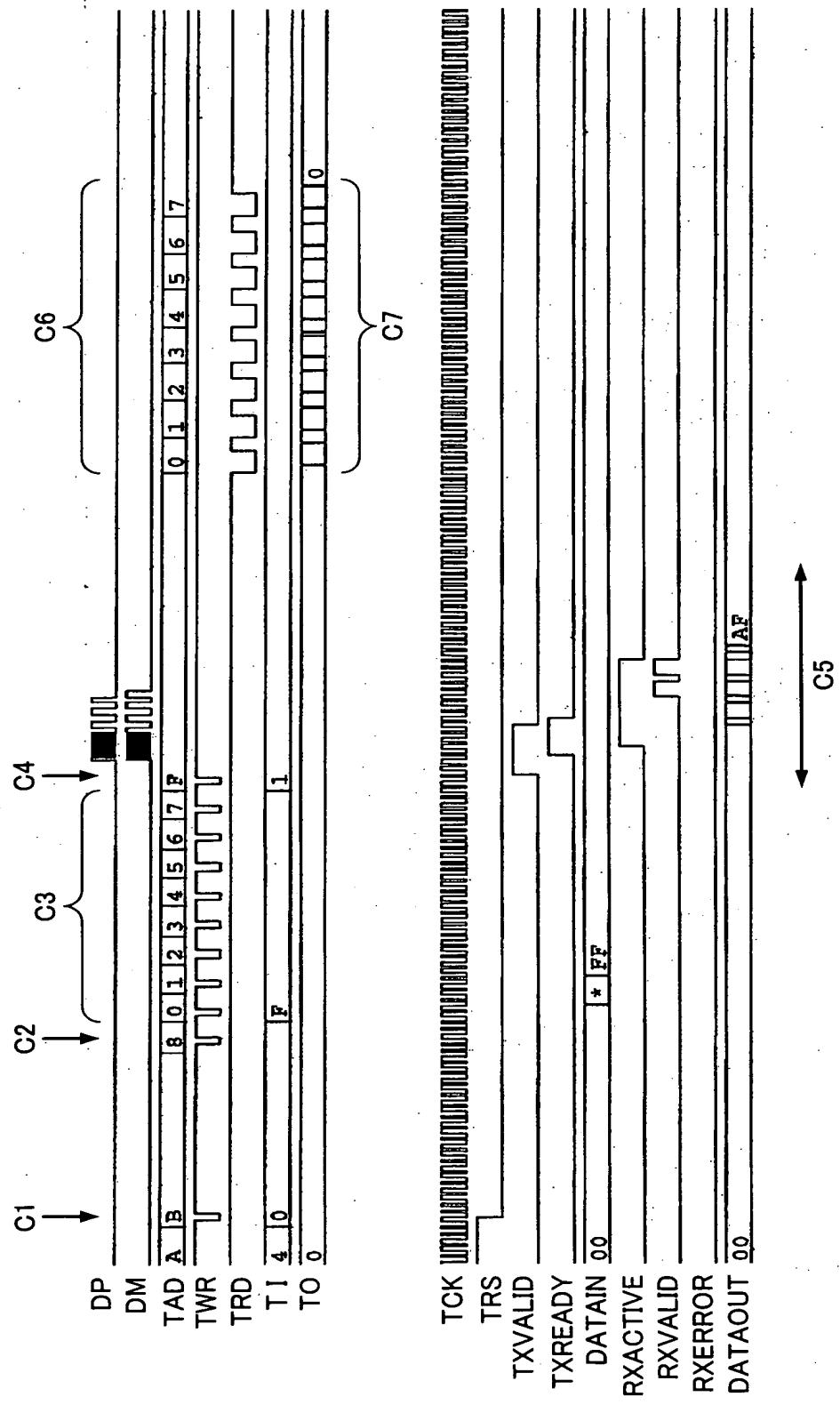


FIG. 14

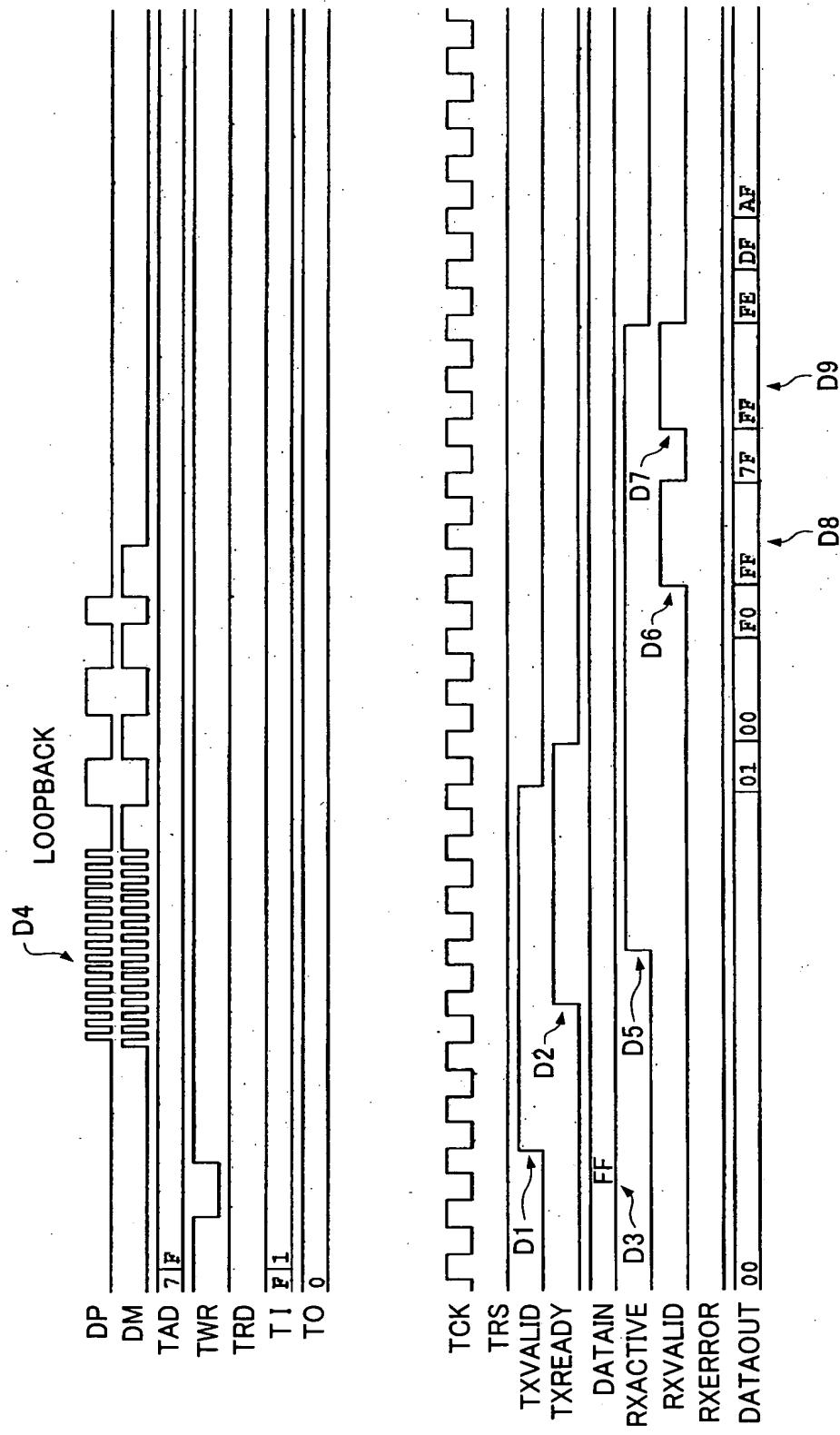


FIG. 15

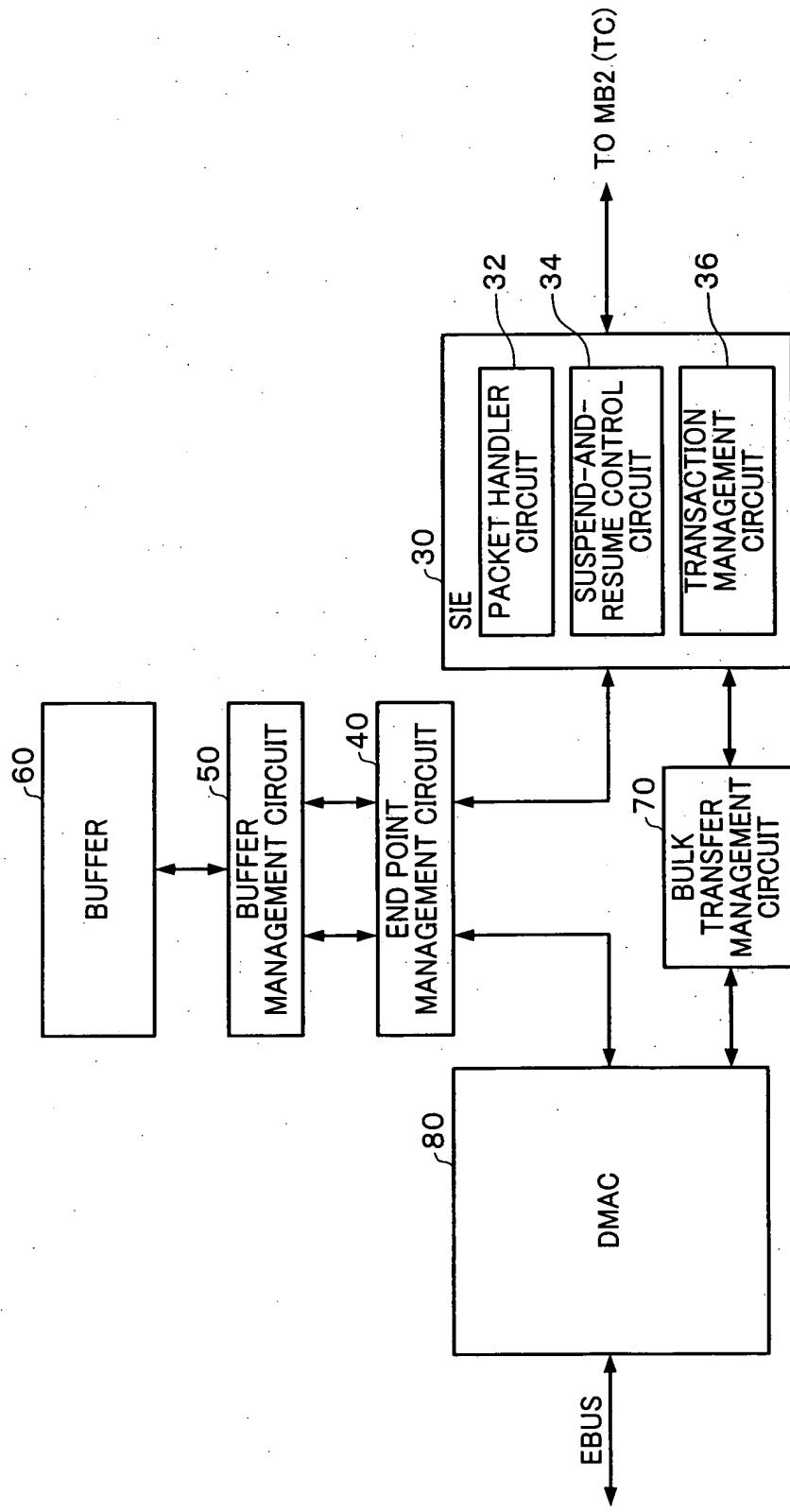


FIG. 16

